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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/586,191
	Filing Date	June 2, 2000
	First Named Inventor	Adrian J. Isles
	Art Unit	2123
	Examiner Name	Sharon, Ayal I.
Total Number of Pages in This Submission	Attorney Docket Number	AVER-01003US0

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Firm or Individual name	David E. Cromer, Vierra Magen Marcus Harmon & DeNiro LLP
Signature	<i>David E. Cromer</i>
Date	September 30, 2004

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		FUJITA, et al., "Speeding Up Look-Up-Table Driven Logic Simulation", VLSI 1999, pp 1-13.	
		FUJITA, et al., "Logic Synthesis for a Single Large Look-up Table", ICCD 1995, hand annotated pp 1-10.	
		SHOSTAK, Robert, E. "A Practical Decision Procedure for Arithmetic with Functional Systems", Journal of the Association for Computing Machinery, April 1979, pp 351-360, Vol. 26, No. 2.	
		SRIVAS, et al., "Formal Verification of a Pipelined Microprocessor", IEEE Software, September 1990, pp 52-64, Vol. 7, No. 5.	
		BURCH, et al., "Automatic Verification of Pipelined Microprocessor Control", Proceedings of the 6th International Conference on Computer Aided Verification, June 1994, pp 68-80.	
		HOJATI, et al., "Automatic Datapath Abstraction in Hardware Systems", Proceedings of the 7th International Conference on Computer Aided Verification, July 1995, pp 98-113.	
		HOJATI, et al., "Verification Using Uninterpreted Functions and Finite Instantiations", Proceedings of the First International Conference on Formal Methods in Computer-Aided Design, November 1996, pp 218-232,	
		ISLES, et al., "Computing Reachable Control States of Systems Modeled with Uninterpreted Functions and Infinite Memory", Proceedings of the 10th International Conference on Computer-Aided Verification, July 1998, pp 256-267.	
		BRAYTON, et al. "VIS: A System for Verification and Synthesis", The VIS Group, In the Proceedings of the 8th International Conference on Computer Aided Verification, Springer Lecture Notes in Computer Science, #1102, J	

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